# ICICC-2020
# International Conference on Innovative Computing and Communication
**Organized by Shaheed Sukhdev College of Business Studies, New Delhi, India**
**On 21-23rd Feb 2020.**

## ********** CALL FOR PAPERS **********

### SPECIAL SESSION ON
**VLSI Design , Embedded Systems and Technologies in the era Secure and Connected World utilizing Internet of Everything (IoE) and the Cloud Computing**

### PUBLICATION POLICIES :
**All the accepted papers (after double blinded peer review) are published by Springer AISC series (ISI Proceedings, EI-Compendex, DBLP, SCOPUS, Google Scholar and Springerlink).**

**Extended selected papers will be published in the special issues of SCI/SCOPUS/WoS/DBLP/ACM indexed Journals.**

### SESSION ORGANIZERS:
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### IMPORTANT DATES:

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| Deadline For Manuscript Submission | October 1st, 2019 |
| Notification of Acceptance / Rejection | November 30th, 2019 |
| Final Manuscript Due | December 31st, 2019 |
| Registration deadline | January 10th, 2020 |
| Conference Date | February 21st, 2020 |

### ADVISORY/EDITORIAL BOARD:
**Dr Hari Chauhan, Analog Devices Inc, USA**
**Prof. (Dr.) C.S. Rai, GGSIPU, New Delhi, India**
**Prof. (Dr.) Pravin Chandra, GGSIPU, New Delhi, India**
**Dr Manoj Kumar Taleja, Associate Professor, GGSIPU, New Delhi, India**

### SESSION DESCRIPTION:
**The main objective of this session is to provide the platform to the researchers, industry experts, academicians and innovative individuals to get together and discuss the all Emerging trends in IC design technologies in the era of secure and connected world. In the technology enabled world, interconnecting devices plays major role and hence the IOE aiming to augment the human life driven with the advances in hardware capabilities. For many such applications the circuits/systems need special emphasis in design stages targeting cloud computing and IOE. The platform hence also tries to collate efforts in VLSI and Embedded architectures, circuit and applications for IOE and cloud computing.**

### RECOMMENDED TOPICS:
**Topics to be discussed in this special session include (but are not limited to) the following:**

**System-level design methodologies, processor design, memory design, multicore systems, GPU design, on-chip communication architectures, networks-on-chip, performance analysis, defect-tolerant architectures, accelerators foremerging workloads (e.g., machine learning)**

**Communication systems, Digital signal processing (DSP), VLSI signal processing, Adaptive Signal Processing, Advances in Digital Design, Logic, physical synthesis, place and route, clock tree design, physical verification, timing and signal integrity, power integrity, design for manufacturability, design for yield, variation-tolerant design, design challenges for advanced technology nodes, Performance optimization methodologies**

**Analog, Mixed-Signal, and RF Design, high-speed wired and wireless communication interfaces, low-power analog and RF, memory design, standard cell design Power-Aware Design, Power analysis and estimation, power optimization, energy-efficient design, thermal management, battery-aware design, energy harvesting**

**CMOS Technology and Devices, Deep nanoscale CMOS devices, device modeling and simulation, device/circuit-level reliability and variability models, New device/ transistor models and their characterization, Emerging Technologies, MEMS, CMOS sensors, design methodologies for nanotechnology, biomedical circuits, carbon nanotube-based computing, spintronics, silicon photonics, neuromorphic computing**

**FPGA Design and Reconfigurable Systems, Reconfigurable computing, FPGA architecture and FPGA circuit design, CAD for FPGA, FPGA prototyping, FPGA-based accelerators for cloud servers, Biomedical , Wireless Systems, Wireless sensor networks, low-power wireless systems, wireless protocols, wireless power delivery, Artificial Intelligence concepts and their applications in VLSI Fuzzy and other techniques and their application in VLSI**

**Embedded Systems Hardware, Hardware/Software co-design, embedded SoC, embedded multi-core systems, board-level hardware, hardware platforms for Internet-of-Things (IoT) devices**

**Design Verification, Functional verification, behavioral and RTL simulation, coverage-driven verification, assertion-based verification, emulation, hardware-assisted verification, formal verification, equivalence checking Test, Reliability, and Fault-Tolerance, DFT, fault modeling and simulation, ATPG, BIST, repair, delay test, fault tolerance, AMS/RF test, board-level and system-level test, silicon debug, post-silicon validation, memory test, reliability testing, defect and fault recoverability.**

**Computer-Aided Design (CAD) tools, logic mapping, simulation and formal verification, layout (partitioning, placement, routing, floor planning,compaction), Futuristic development and optimization tools**

**Applications in Healthcare, Smart Grid, Intelligent and Secure Transportation Systems, Safety Assurance of Embedded Circuits and Systems, Secure Embedded Circuits and Systems**

## SUBMISSION PROCEDURE:

**Researchers and practitioners are invited to submit papers for this special theme session on "VLSI Design, Embedded Systems and Technologies in the era Secure and Connected World utilizing Internet of Everything (IoE) and the Cloud Computing" *on or before* 5th December 2019. All submissions must be original and may not be under review by another publication. INTERESTED AUTHORS SHOULD CONSULT THE CONFERENCE'S GUIDELINES FOR MANUSCRIPT SUBMISSIONS at http://icicc-conf.com/paper_submission.html. All submitted papers will be reviewed on a double-blind, peer review basis.**

## IMPORTANT LINKS/FURTHER DETAILS

**http://icicc-conf.com/**
**http://icicc-conf.com/new_special_session**

**NOTE:** While submitting paper in this special session, please specify **"VLSI Design , Embedded Systems and Technologies in the era Secure and Connected World utilizing Internet of Everything (IoE) and the Cloud Computing"** at the top (above paper title) of the first page of your paper.

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